WHAT IS CLAIMED IS:

1. A charge pump comprising:

a first PMOS transistor;

a first NMOS transistor coupled to the first PMOS transistor via a first common drain node;

a second PMOS transistor;

a second NMOS transistor coupled to the second PMOS transistor via a second common drain node;

a first current source coupled to respective source terminals of the first and second PMOS transistors;

a second current source coupled to respective source terminals of the first and second NMOS transistors;

a first operational amplifier having a first input coupled to the first common drain node and a second input coupled to the second common drain node;

a reference circuit; and

a second operational amplifier having a first input coupled to the first common drain node and a second input coupled to the reference circuit.

2. The charge pump of claim 1, further comprising a capacitor coupled to the first common drain node.

3. The charge pump of claim 1, wherein the reference circuit includes:

a third PMOS transistor;

a third NMOS transistor coupled to the third PMOS transistor via a third common drain node;

a third current source coupled to a source terminal of the third PMOS transistor; and

a fourth current source coupled to a source terminal of the third NMOS transistor;

wherein the second input of the second operational amplifier is coupled to the third common drain node.

4. The charge pump of claim 1, wherein the first current source is a PMOS current source.

5. The charge pump of claim 1, wherein the second current source is an NMOS current source.

6. The charge pump of claim 1, wherein an output of the first operational amplifier is coupled to the second common drain node.

7. The charge pump of claim 1, wherein an output of the second operational amplifier is coupled to a gate terminal of the first current source.

8. An apparatus comprising:

a communication port; and

a serializer/deserializer coupled to the communication port, the serializer/deserializer including a phase locked loop, the phase locked loop including a charge pump, the charge pump including:

a first PMOS transistor;

a first NMOS transistor coupled to the first PMOS transistor via a first common drain node;

a second PMOS transistor;

a second NMOS transistor coupled to the second PMOS transistor via a second common drain node;

a first current source coupled to respective source terminals of the first and second PMOS transistors;

a second current source coupled to respective source terminals of the first and second NMOS transistors;

a first operational amplifier having a first input coupled to the first common drain node and having a second input and an output both coupled to the second common drain node;

a reference circuit; and

a second operational amplifier having a first input coupled to the first common drain node, a second input coupled to the reference circuit, and an output coupled to a gate terminal of the first current source.

9. The apparatus of claim 8, wherein the charge pump further includes a capacitor coupled to the first common drain node.

10. The apparatus of claim 8, wherein the reference circuit includes:

a third PMOS transistor;

a third NMOS transistor coupled to the third PMOS transistor via a third common drain node;

a third current source coupled to a source terminal of the third PMOS transistor; and

a fourth current source coupled to a source terminal of the third NMOS transistor;

wherein the second input of the second operational amplifier is coupled to the third common drain node.

11. The apparatus of claim 8, wherein the first current source is a PMOS current source.

12. The apparatus of claim 8, wherein the second current source is an NMOS current source.

13. The apparatus of claim 8, wherein an output of the first operational amplifier is coupled to the second common drain node.

14. The apparatus of claim 8, wherein an output of the second operational amplifier is coupled to a gate terminal of the first current source.

15. A charge pump comprising:

an input differential pair including a first transistor and a second transistor;

a first current mirror coupled to a drain terminal of the second transistor via a common drain node;

a second current mirror coupled to the first current mirror and coupled to an output terminal of the charge pump to selectively discharge the output terminal; and

a third current mirror coupled as a load to the first transistor and coupled to the common drain node to selectively pull up the common drain node.

16. The charge pump of claim 15, wherein the first current mirror is formed of PMOS devices.

17. The charge pump of claim 15, wherein the second current mirror is formed of NMOS devices.

18. The charge pump of claim 15, wherein the third current mirror is formed of PMOS devices.

19. The charge pump of claim 15, further comprising a capacitor coupled to the output terminal.

20. An apparatus comprising:

a communication port; and

a serializer/deserializer coupled to the communication port, the serializer/deserializer including a phase locked loop, the phase locked loop including a charge pump, the charge pump including:

an input differential pair including a first transistor and a second transistor;

a first current mirror coupled to a drain terminal of the second transistor via a common drain node;

a second current mirror coupled to the first current mirror and coupled to an output terminal of the charge pump to selectively discharge the output terminal; and

a third current mirror coupled as a load to the first transistor and coupled to the common drain node to selectively pull up the common drain node.

21. The apparatus of claim 20, wherein the first current mirror is formed of PMOS devices.

22. The apparatus of claim 20, wherein the second current mirror is formed of NMOS devices.

23. The apparatus of claim 20, wherein the third current mirror is formed of PMOS devices.

24. The apparatus of claim 20, further comprising a capacitor coupled to the output terminal.